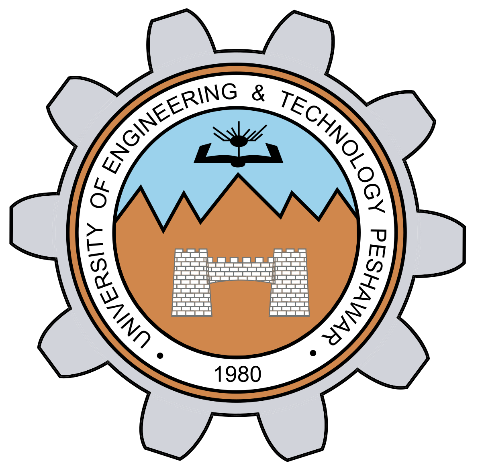
**Lab 04**



**Spring 2023**

**DSD-Lab**

**Submitted by**:

**Maaz Habib**

**Registration NO:**

**20PWCSE1952**

**Class Section:**

C

“On my honor, as a student of University of Engineering and Technology I have neither given nor received unauthorized assistance on this academic work”

**Submitted to:**

Engr Muhammad Usman

**Date:**

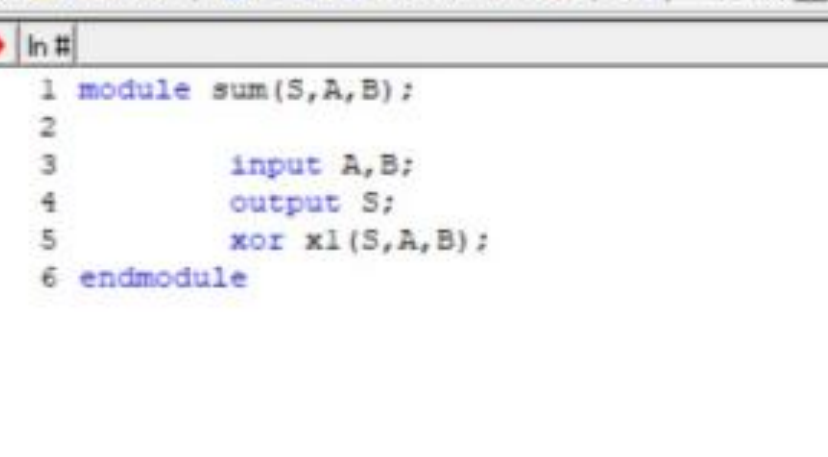
Sunday April 4,2023

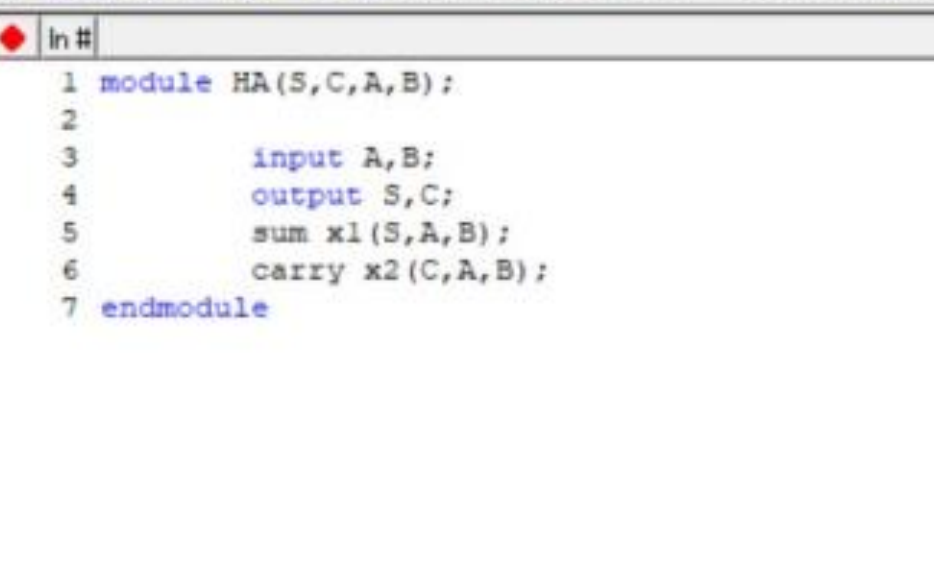
Department of Computer Systems Engineering

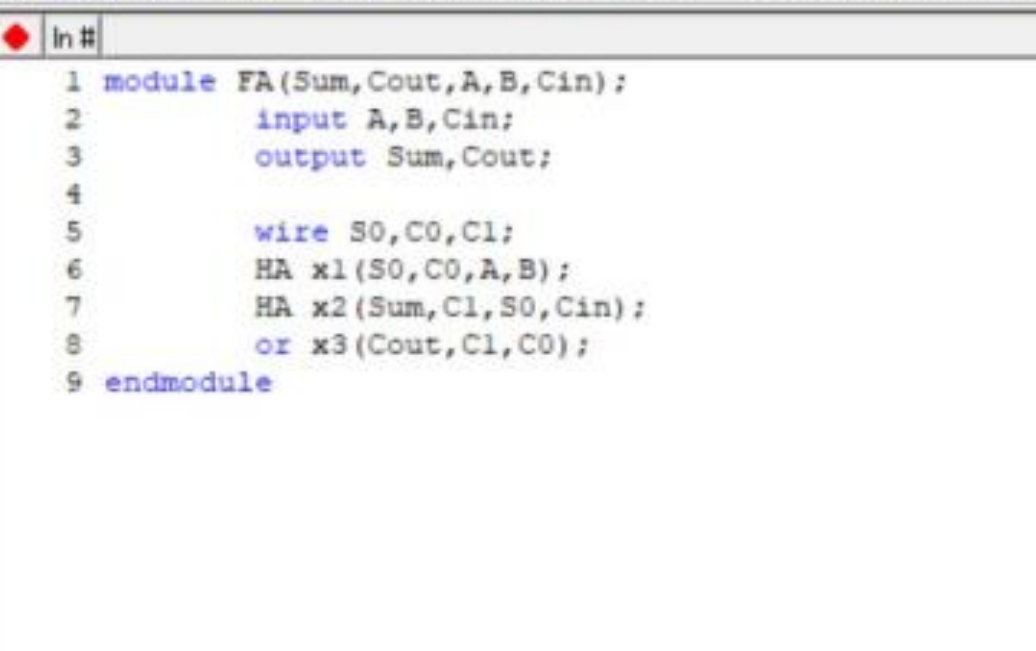
University of Engineering and Technology, Peshawar

**Lab Task:**

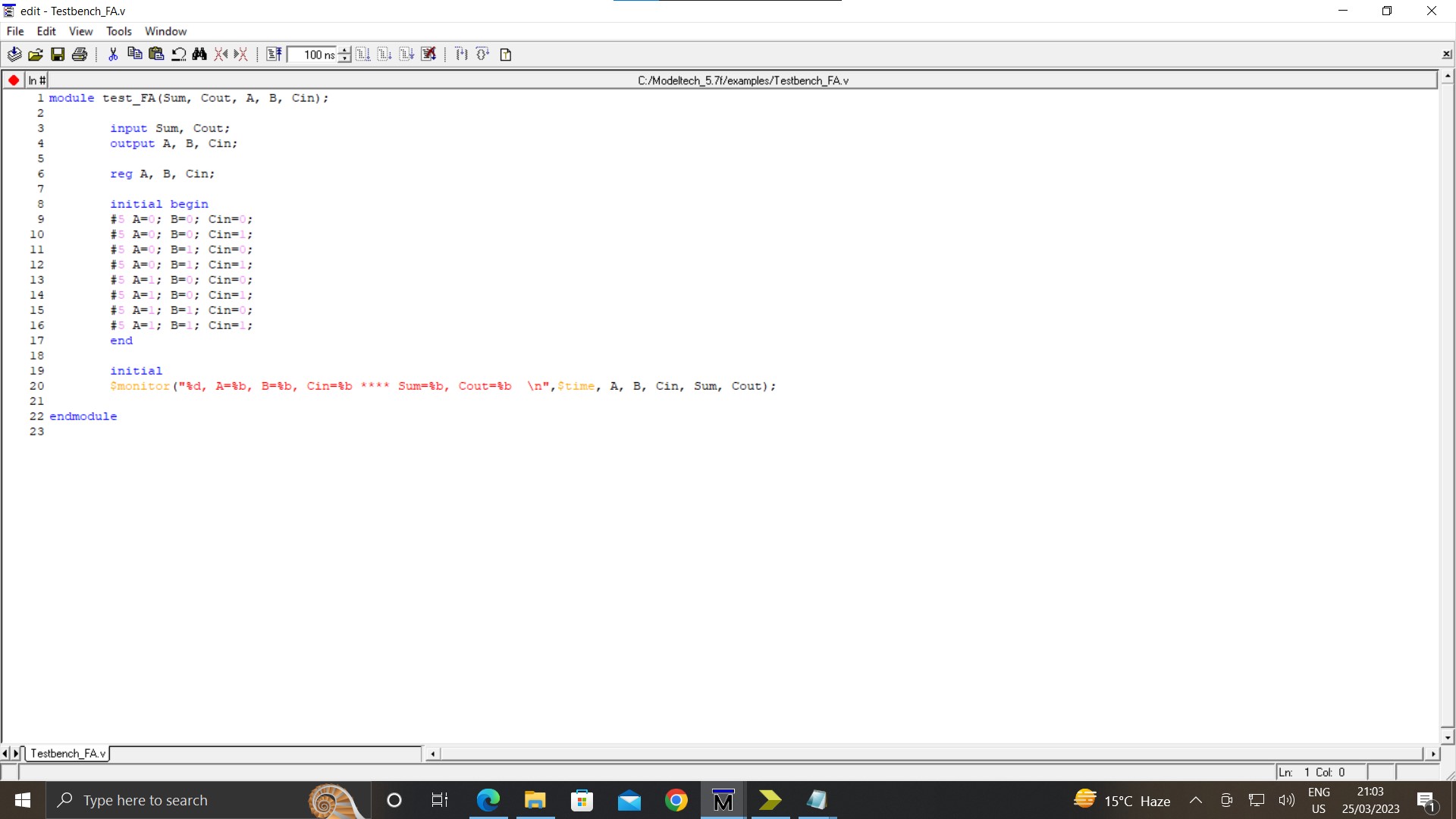
The following steps should be performed while designing a 4 bit RCA adder ModelSim:

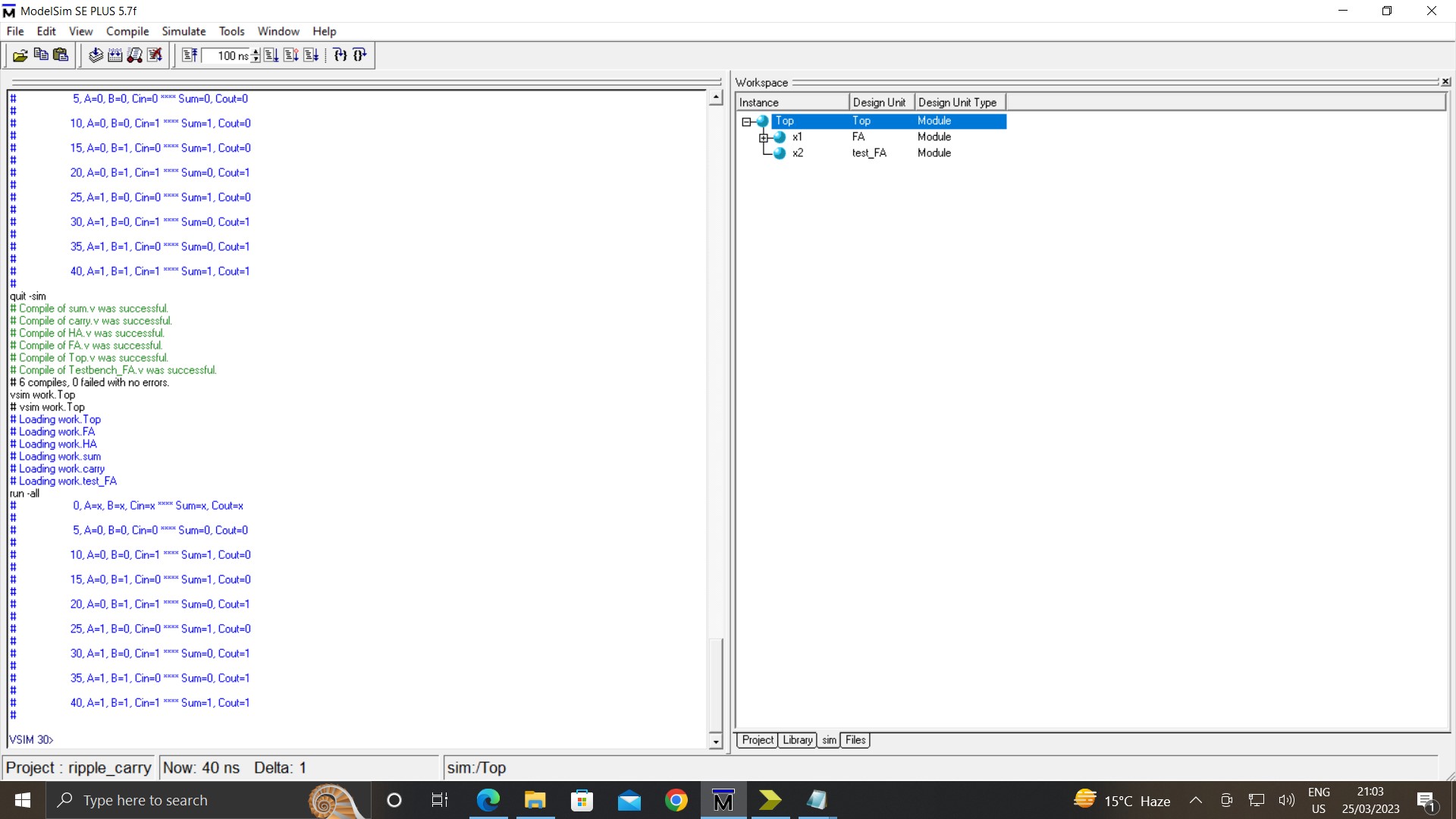
1. First implement a Full adder using data flow/gate level modeling.

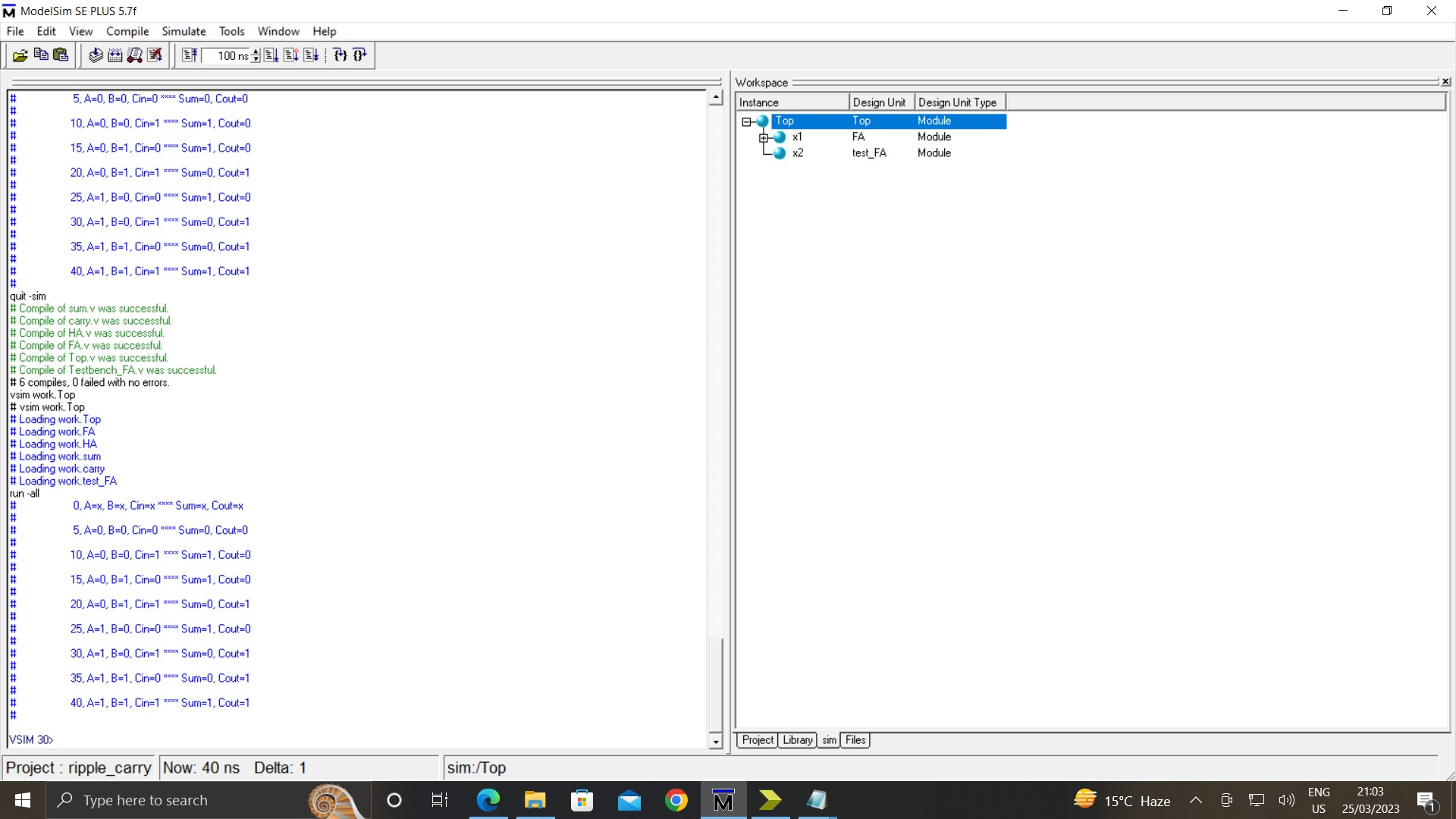




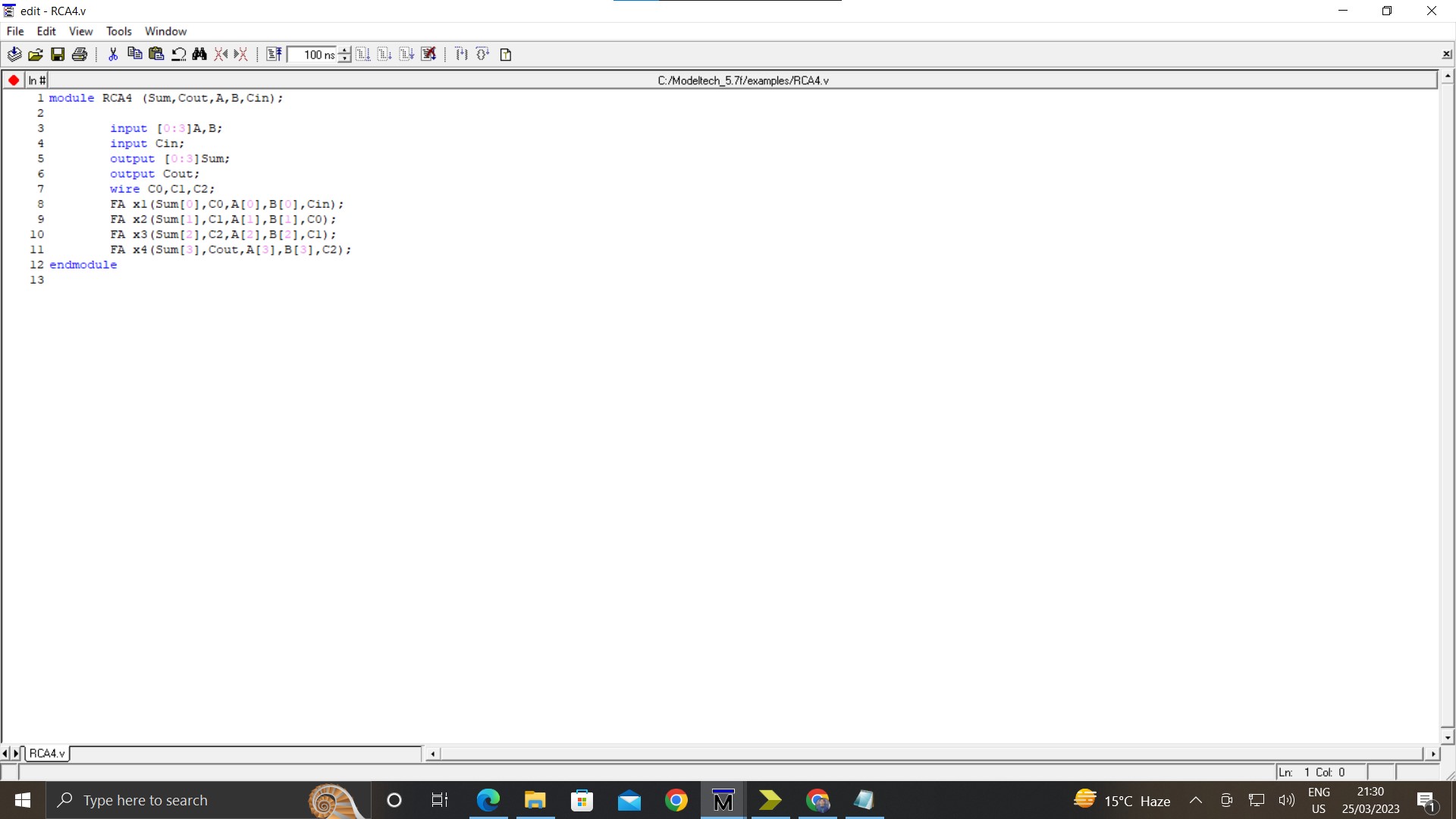
1. **Simulate the Full adder with a test bench.**



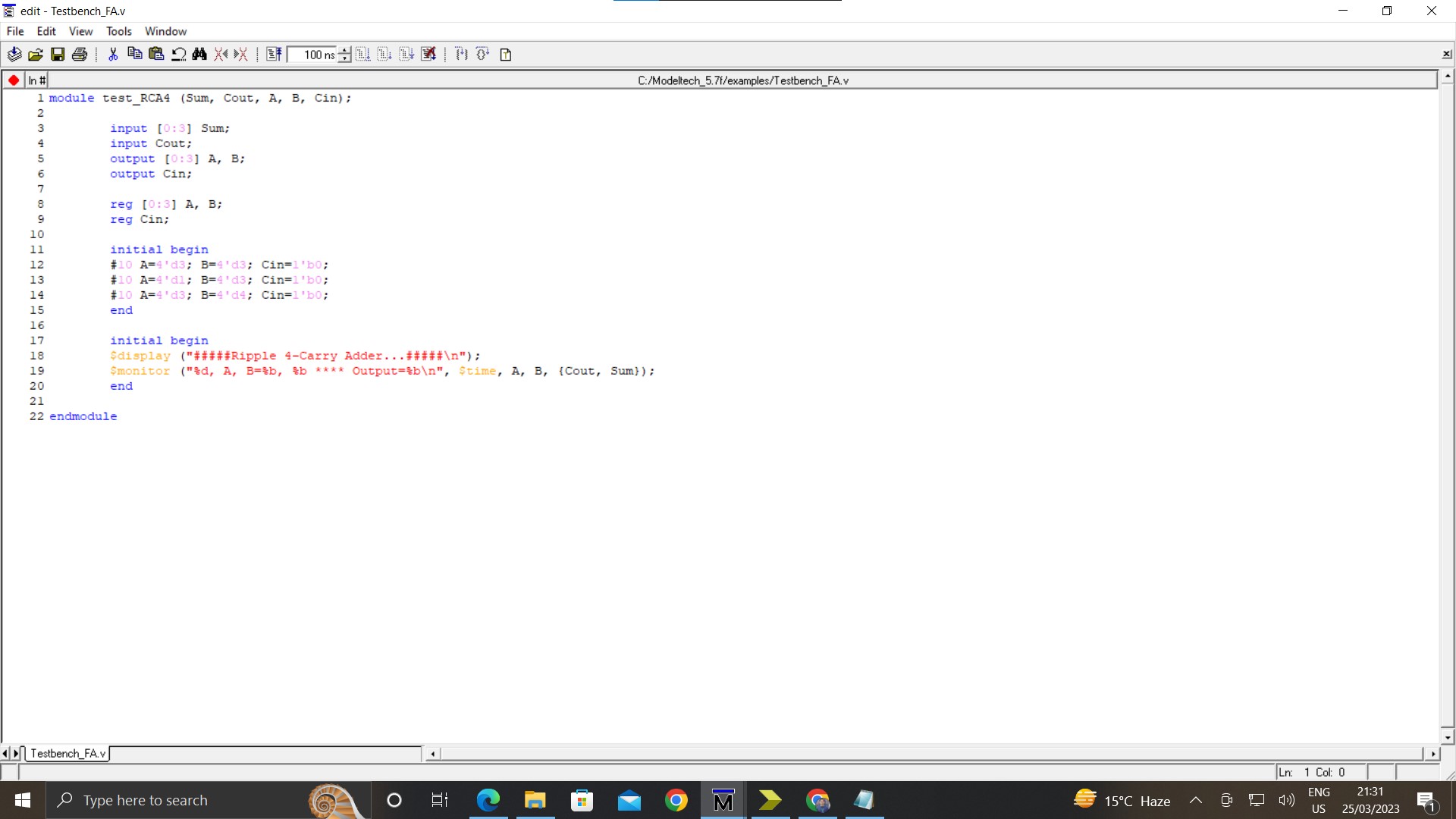


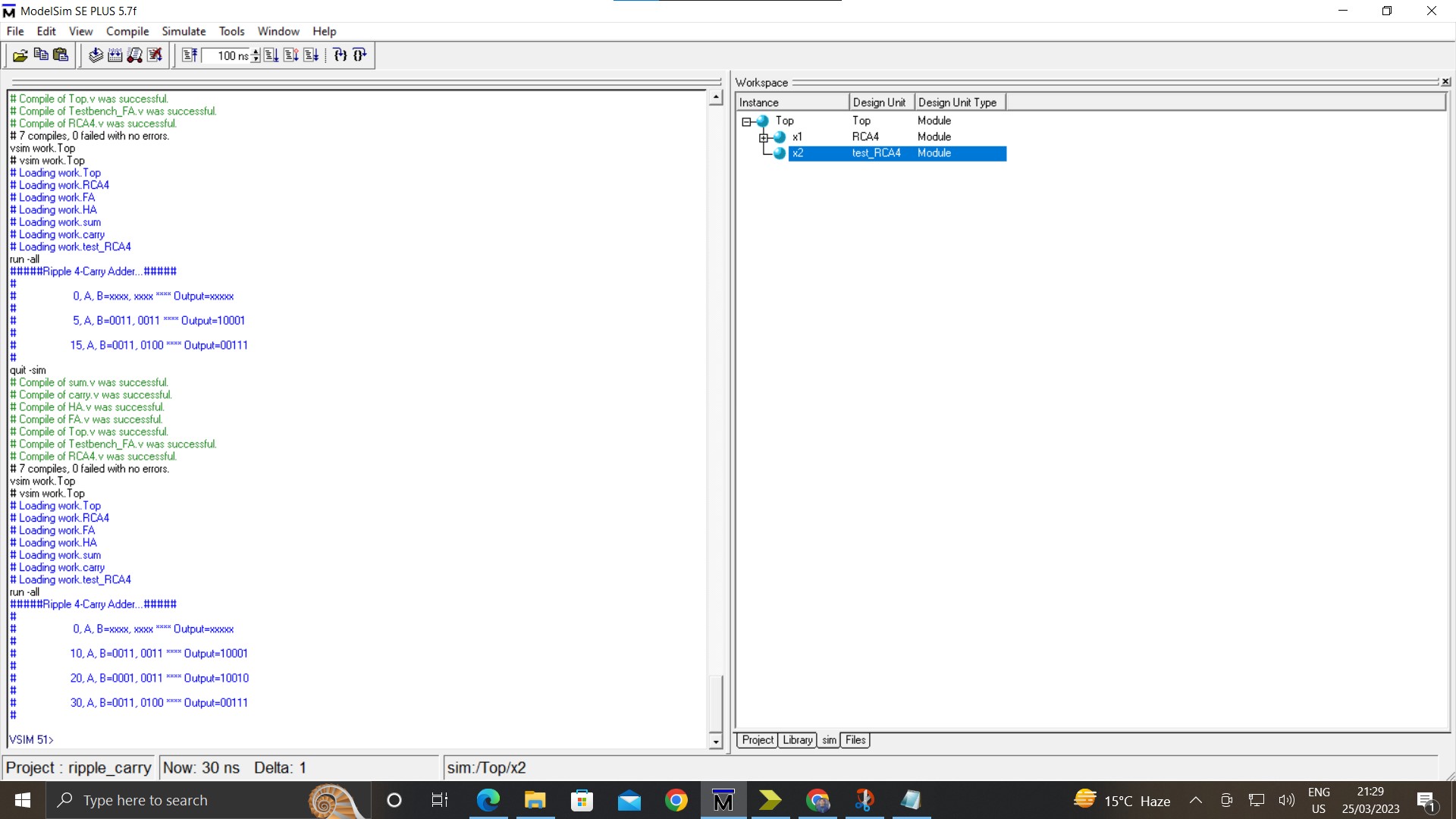


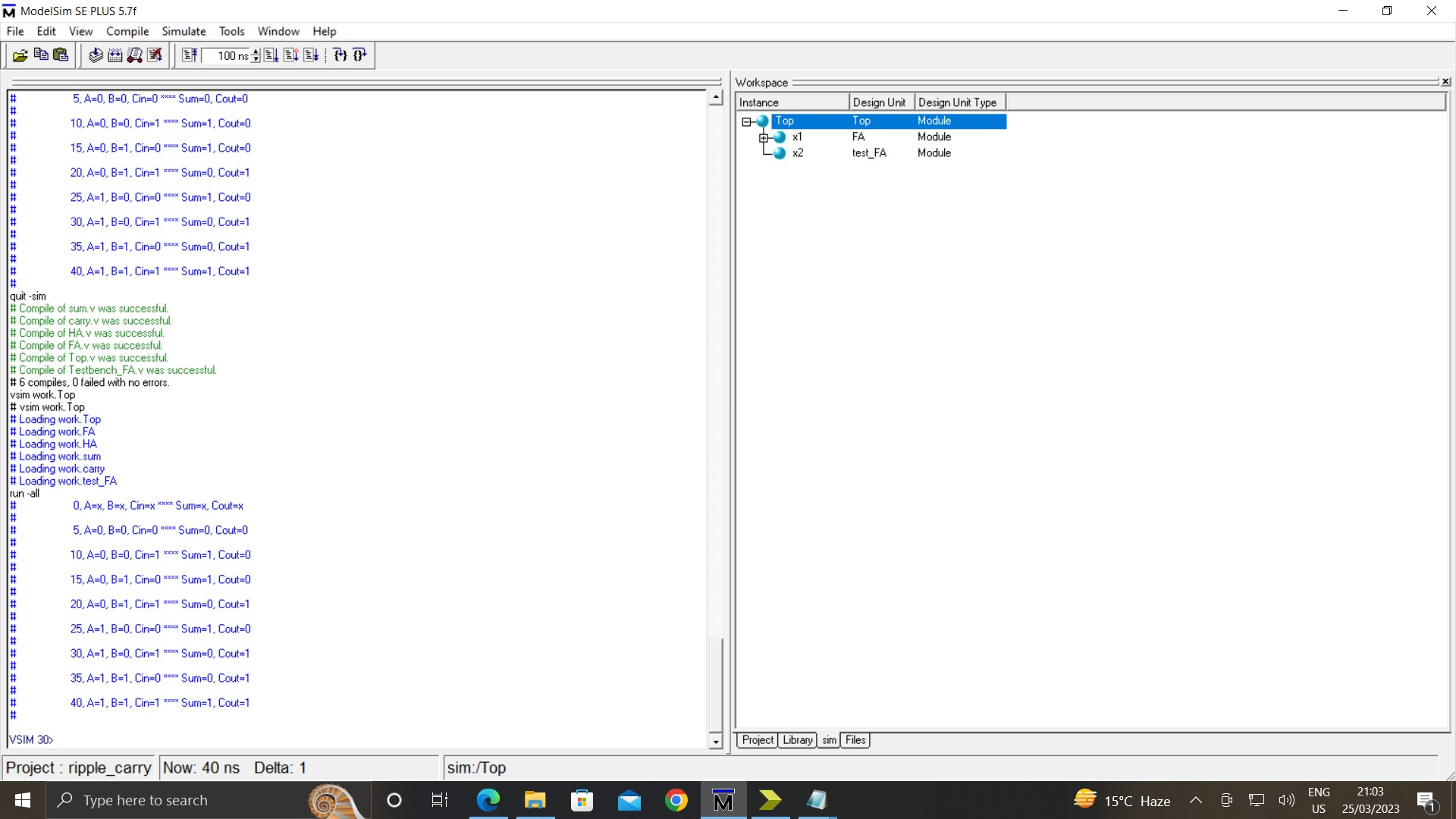
1. Instantiate the Full adder four times and connect the circuit as shown.



1. **Now again write a test bench and simulate the 4 bit RCA.**

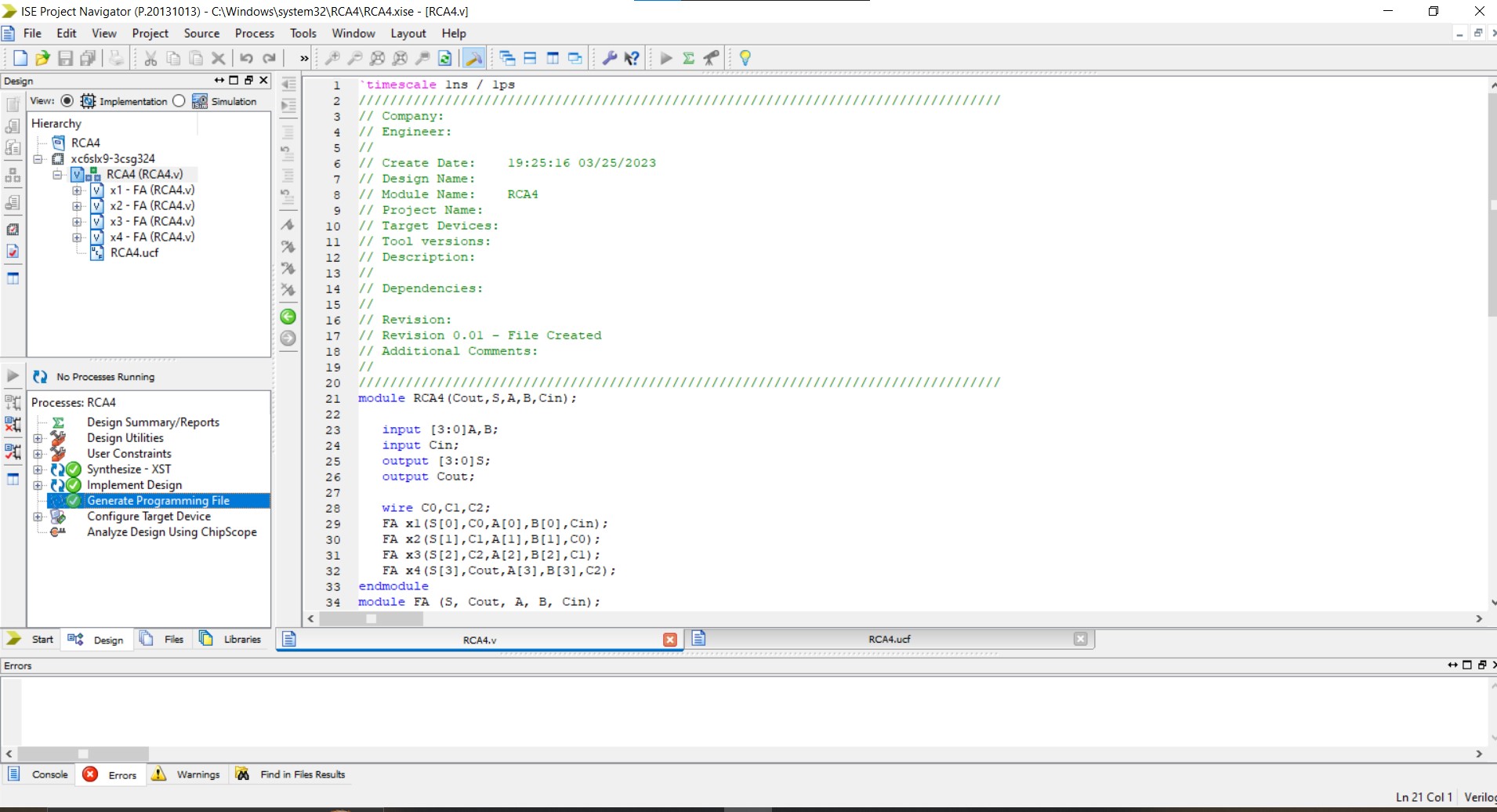


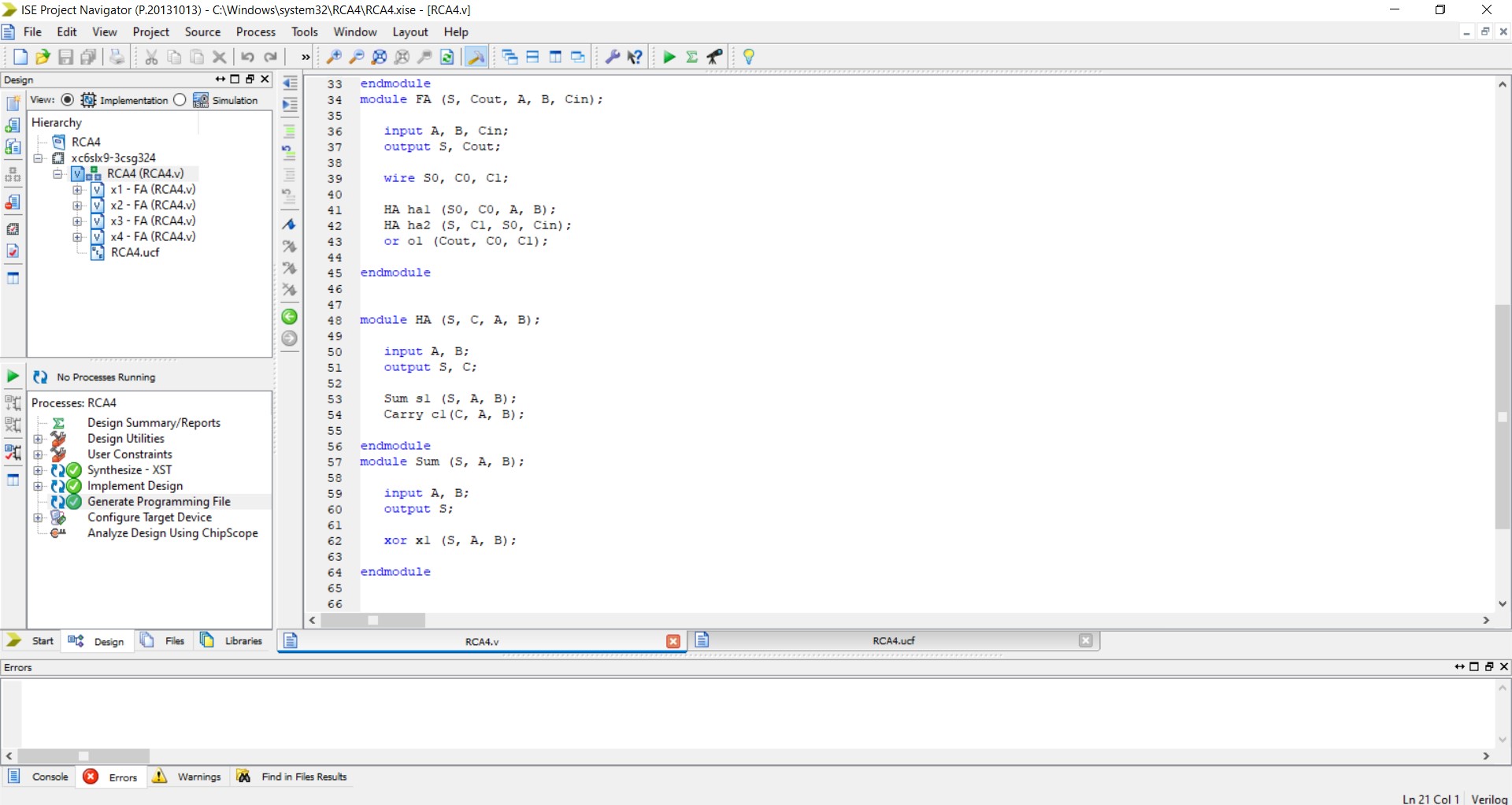




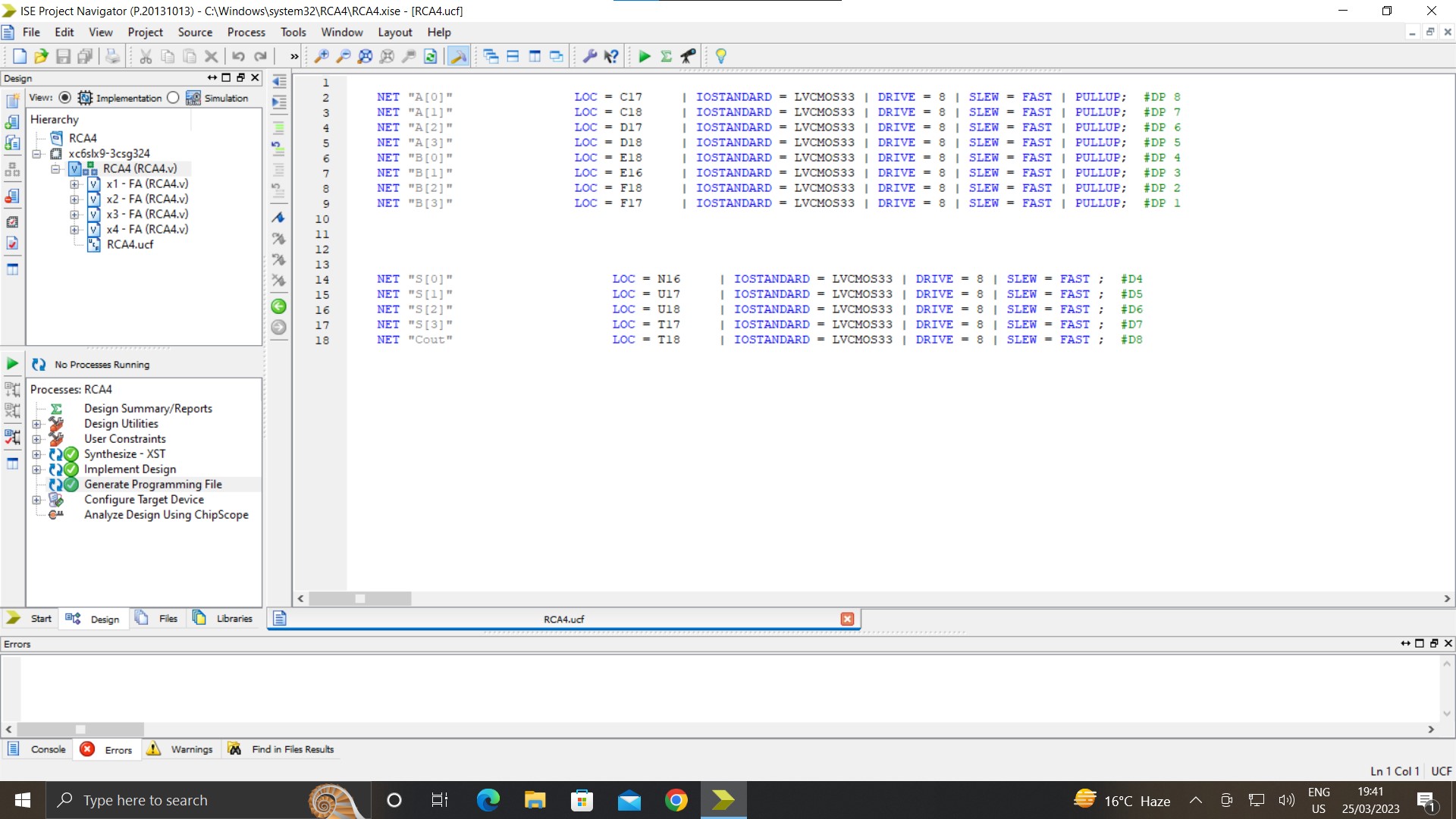
**Xilinx:**

1. **Make new project in Xilinx and add the files that you simulated in ModelSim.**





1. **Add User Constraint File inputs should be locked with the switches, C0 should be permanently “0” while S0-S4 and C4 with LEDS**



⇒**In Lab we Implement the code on FPGA:**

Write RCA4.bin on FPGA:

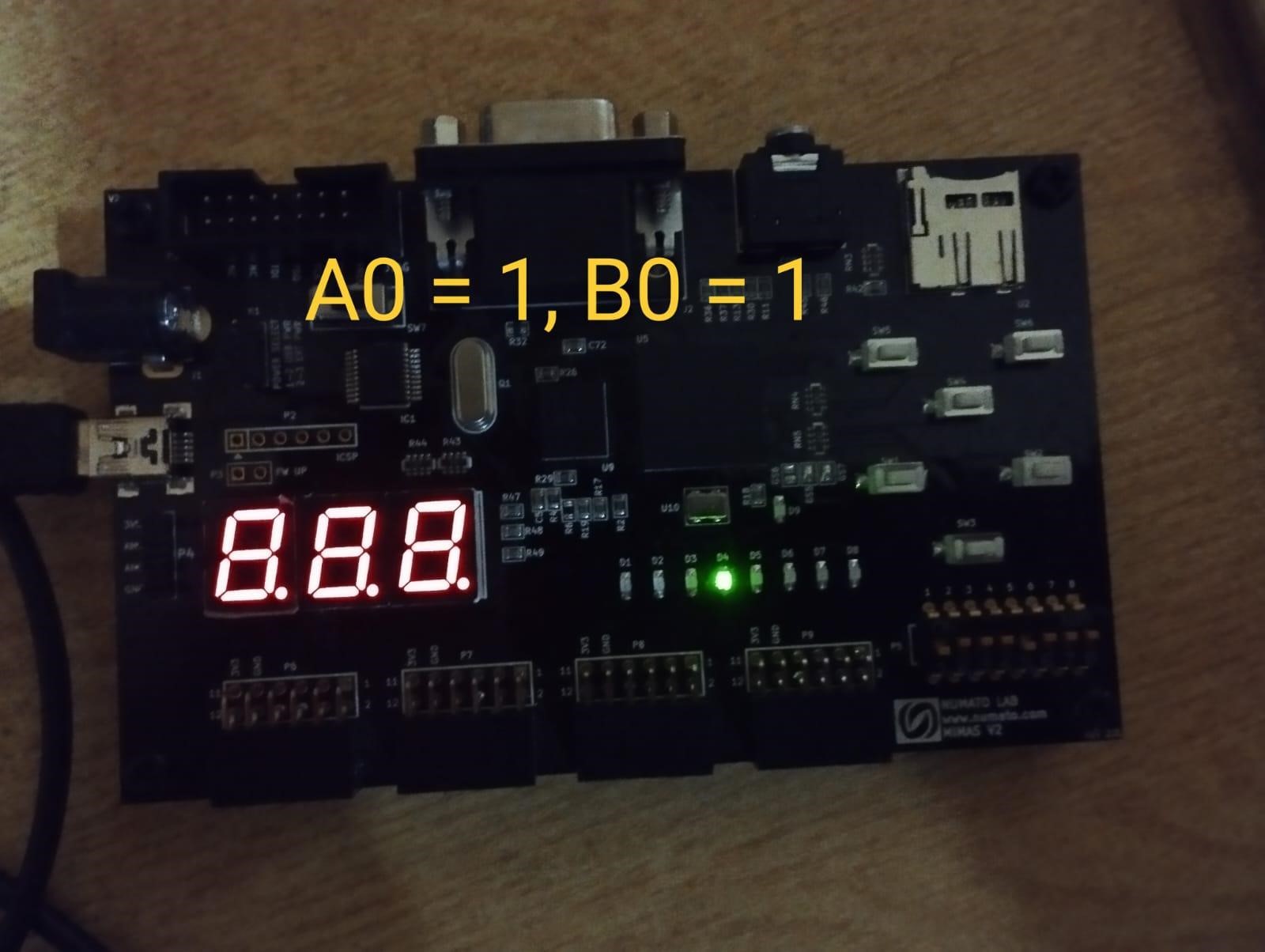
Here is Screenshots Attached Below of lab perform:

Labels are added in the pic that which one is on and off:

**A0 IS ON:**



**A0=1 B0=1:**



**All on:**

